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Phase-lock Loop Design in Digital Receiver

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Abstract **- This paper presents the design of phase-lock loop in which composed of voltage control oscillator (VCO), loop filter, phase detector and prescalar. Design and development of local oscillator (LO) module which delivers 12.5 MHz to 39 MHz and mixer for IF-DSP receiver are presented. The mixer receives the RF ranging from 3 MHz to 30 MHz and produces output frequency 9MHz IF. The PLL (phase-lock loop) module is constructed by using 64 HCMOS divider (CMOS 4046), and LM 358 operational amplifier which is working as a level translator for the voltage control oscillator (VCO) control voltage and loop filter. The frequency range of local oscillator is considered from 12.5 to 39 MHz in 500 kHz steps and its output level is +17 dBm ± 2 dBm. This module has frequency stability of ± 20 Hz over - 10 to +50˚C. But its phase noise is less than or equal to - 132 dBc /Hz.**

Keywords- **voltage control oscillator, loop filter, phase detector, prescalar, PLL module**

I. INTRODUCTION

Phase-lock loops are used in a wide variety of communication system applications. The PLL is a very interesting and useful building block available as single integrated circuits represents a blend of digital and analog techniques all in one package. One of its many applications and features is tone-decoding. There has been traditionally some reluctance to use PLL's, partly because of the complexity of discrete PLL circuits.

The PLL is an electronic feedback circuit. It is capable of locking onto or synchronizing with and incoming signal. When the phase changes, indicating that the incoming frequency is changing, the phase detector's output voltage (error voltage) increases or decreases just the enough to keep the oscillator frequency the same as the incoming frequency.

II. PHASE-LOCK LOOP SYSTEM

Phase-Locked Loop is basically a closed loop frequency control system, which functioning is based on the phase sensitive detection of phase difference between the input and output signals of the controlled oscillator.

A PLL has three core components. They are Phase Detector (PD) or the multiplier, Loop filter (LF) and Voltage controlled Oscillator or VCO. The PLL is as reliable a circuit element as an op-amp or flip-flop. The phase detector is a device that compares two input frequencies, generating an output that is a measure of their phase difference. If f_{IN} doesn't equal to f_{VCO}, the phase-error signal, after being filtered and amplified, causes the VCO frequency to deviate in the direction of f_{IN}. If conditions are right, the VCO will quickly "lock" to f_{IN} maintaining a fixed relationship with the input signal.

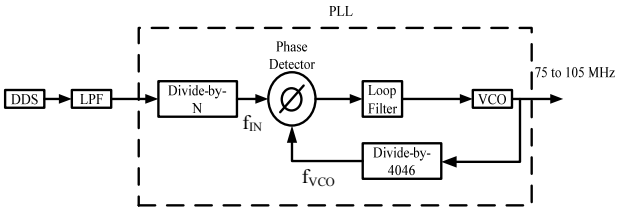

Fig. 1 Block diagram of phase-lock loop

When there is no input signal, error voltage is zero and the frequency, f_{VCO}, of the voltage-controlled oscillator is called the free-running of center frequency. When an input signal is applied, the phase detector compares the phase and frequency of the input signal with the VCO frequency and produces error voltage. This error voltage is proportional to the phase and frequency difference of the incoming frequency and the VCO frequency. The low-pass filter passes only the difference frequency which is the lower of the two components. This signal is amplified and fed back to the VCO as a control voltage. The control voltage forces the VCO frequency to change in a direction that reduces the difference between the incoming frequency and VCO frequency. When these frequencies are sufficiently close in value, the feedback action of the PLL causes the VCO to lock onto the incoming signal. Once the VCO locks, its frequency is the same as the input frequency with a slight difference in phase. This phase difference is necessary to keep the PLL in the lock condition.

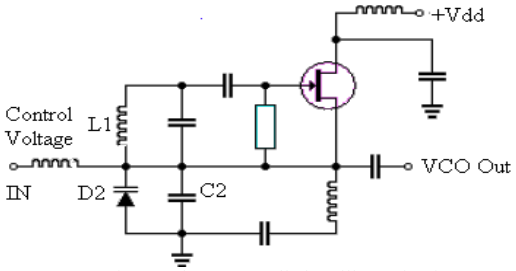

Fig. 2 Voltage-controlled oscillator circuit

A voltage controlled oscillator is described in Fig. 2**.** It shows a voltage controlled oscillator by which frequency of oscillation is determined by L_1, C_2, and D_2. D_2 is also called varactor or varicap.

Fig. 3 shows that the VCO and Crystal Oscillator outputs are combined with a phase detector and any difference will result in a DC voltage output. This DC voltage is fed back to the Voltage Control Oscillator in such a way that it drives the output of the VCO towards the Crystal Oscillator frequency eventually the VCO will LOCK onto the crystal oscillator frequency.

The crystal frequency was 10 MHz but the VCO to operate on 20 MHz. The phase detector will of course detect a frequency difference and pull the VCO down to 10 MHz. In Fig. 4, a divide-by-four is used instead of the divide-by-two. Then, at LOCK, the VCO would be oscillating at 40 MHz yet still be as stable as the crystal reference frequency. Variable Frequency Oscillator (VFO) is made to change frequency by changing the value of one of the frequency determining circuits.

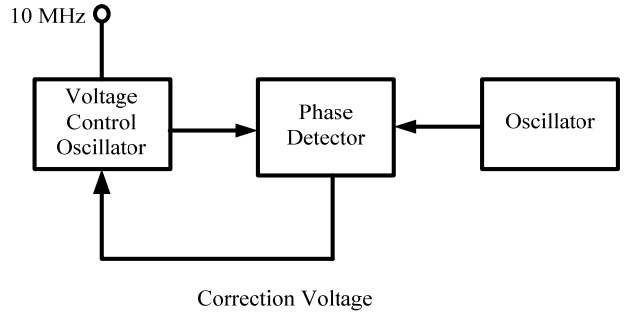

Fig. 3 VCO and crystal oscillator outputs combining with a phase detector

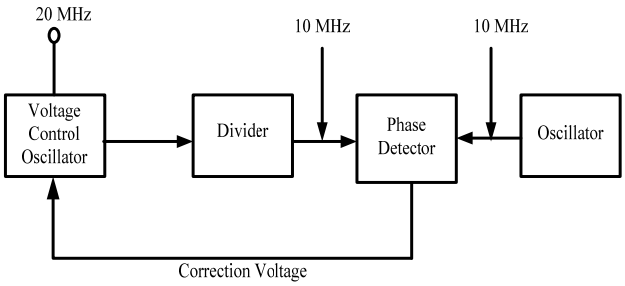

Fig. 4 Using a divide-by-two to operate VCO at 20 MHz with a 10 MHz reference crystal

III. Phase Detector of PLL Components

There are actually two types; one is designed to be driven by analog signals or digital square-wave signals, and another is driven by digital transitions (edges). They are typified by the most common used 565 (linear) and the CMOS 4046, which contains both them.

The simplest phase detector is the digital, which is simply an Exclusive-OR gate. The linear phase detector has similar output-voltage-versus-phase characteristics, although its internal circuitry is actually a "four-quadrant multiplier", also known as a "balanced mixer". Highly linear phase detectors of this type are essential for lock-in detection, which is a fine technique.

The phase detector for digital transitions is sensitive only to the relative timing of *edges* between the signal and VCO input, as shown in Fig. 5. The phase comparator circuit generates either lead or lag output pulses, depending on whether the VCO output transitions occur before or after the transitions of the reference signal, respectively. The width of these pulses is equal to the time between the respective edges. The output circuitry then either sinks or sources current (respectively) during those pulses and is otherwise open-circuited, generating an average output-voltage-versus-phase difference like that in Fig. 6.

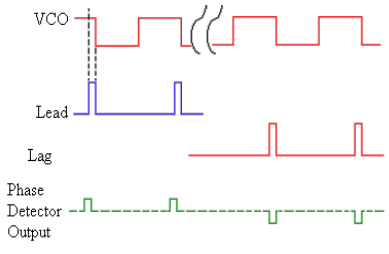

Fig. 5 Relative timing of edges between the signal and VCO input

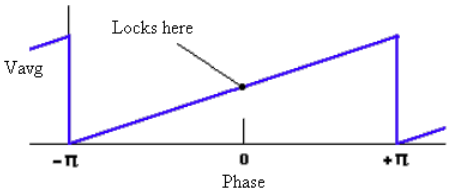

Fig. 6 Average output-voltage-versus-phase difference

IV. Loop Filter of PLL Components

In almost all applications, it will be desirable to filter the signal at the output of the phase detector. A simple lag filter may be used for wide closed loop bandwidth applications such as modulation following where the frequency deviation of the carrier is fairly high (greater than 10%), or where wide-band modulation signals must be followed. For narrow band applications where narrow noise bandwidth is desired, such as applications involving tracking a slowly varying carrier, a lead lag filter should be used. In general the damping factor for the loop becomes quite small resulting in large overshoot and possible instability in the transient response of the loop.

V. CMOS 4046 Phase-Locked Loop Design

A diagram of the 4046 PLL is shown in Fig. 7. The incoming signal V_i goes to the input of an internal amplifier at the chip. The internal amplifier has the input biased at about $+V_{DD}$=2. Therefore, the incoming signal can be capacitive coupled to the input, as shown in Fig. 8. The incoming ac

signal V_i of about one volt peak-to-peak is sufficient for proper operation.

The capacitor C_i together with the input resistance R_i = 100kΩ at the pin 14 form a high-pass filter. C_i should be selected so that V_i is in the pass band of the filter, so that $f_i > 1= (2R_iC_i)$ for the lowest expected frequency f_i of the incoming signal. The output of the internal amplifier is internally connected to one of the two inputs of the phase detector on the chip.

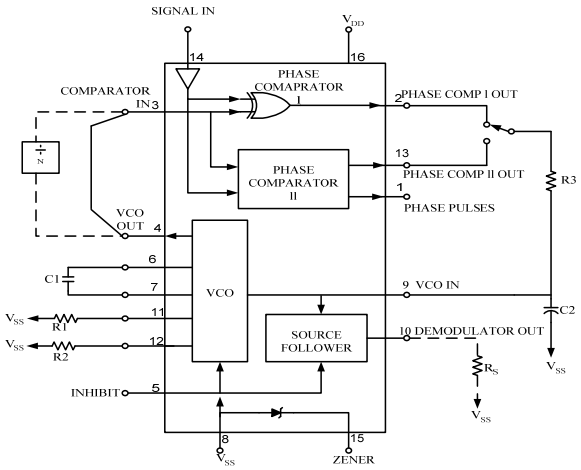

Fig. 7 CMOS 4046 PLL connection diagram

Initially, the operation of the 4046 PLL is no incoming signal at all, V_i = 0. The VCO output V_{osc} is a square-wave signal with 50% duty ratio. Since V_i = 0, the output of the XOR phase detector is exactly the same as the VCO output, $V_\Phi = V_{osc}$. The low-pass filter attenuates ac components of V_Φ so that the filter output is approximately equal to the dc component of V_Φ. In this case, the dc component V_o is equal to V_{DD}=2 because V_Φ is V_{DD} for one half of the period and 0 for the other half of the period. The filter output voltage V_o is the input of the VCO. Therefore, the VCO operates the frequency that corresponds to the voltage $V_o = +V_{DD}$=2 at the VCO input. This frequency is called the center, or the free-running frequency $f_{osc} = f_o$ of the PLL.

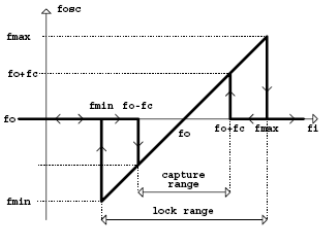

Fig. 8 Steady-state f_{osc} (f_i) characteristic of the PLL

The phase detector on the 4046 is simply an XOR logic gate, with logic low output (V_Φ = 0V) when the two inputs are both high or low, and the logic high output ($V_\Phi = V_{DD}$). In Fig. 9, illustrates the operation of the XOR phase detector when the PLL is in the locked condition. V_1 (the amplified V_i) and V_{osc} (the VCO output) are two phase-shifted periodic square-wave signals at the same frequency $f_{osc} = f_i = 1/T_i$, and with 50% duty ratios. The output of the phase detector is a periodic square-wave signal $V_\Phi(t)$ at the frequency $2f_i$, and with the duty ratio D_Φ that depends on the phase difference Φ between V_i and V_{osc}.

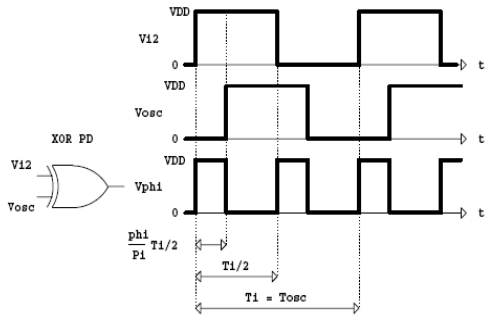

Fig. 9 Operation of the phase detector with XOR gate

The incoming signal V_i at the frequency f_i is brought to the input of the PLL, one of the two inputs of the XOR phase detector. If the frequency f_i is sufficiently closed to the free-running frequency f_o, the PLL will capture the incoming signal. During the capture process, the phase difference between V_i and V_{osc} changes in time, and therefore V_o changes in time until V_o reaches the value required to lock the VCO frequency f_{osc} to the frequency f_i of the incoming signal. In the locked condition $f_{osc} = f_i$, and V_i and V_{osc} are phase shifted by Φ. The phase difference Φ between V_i and V_{osc} depends on the value of the incoming signal frequency f_i.

If $f_i = f_o$, the phase difference must exactly be $\Phi = \pi/2$, $V_o = V_{DD}/2$ and the VCO indeed operates at f_o. If $f_i = f_{max}$, the phase difference Φ must be equal to π in order to obtain $V_o = V_{DD}$ that results in the VCO output frequency equal to f_{max}. It is important to note here that in order to keep $f_{osc} = f_i$ in the locked condition, the filter output voltage V_o must vary together with the frequency f_i of the incoming signal. Therefore, a change in f_i causes a proportional change in V_o, as long as the PLL stays in the locked condition with $f_{osc} = f_i$. As a result, if the incoming signal is frequency modulated, with f_i (t) varying in time, the PLL behaves as an FM demodulator with V_o as the demodulated output.

In this part, close the loop by inserting the RC filter between the phase detector output and the VCO input. Use a pulse generator as the source of the incoming signal V_i. Adjust frequency f_i of V_i to approximately match the free-running frequency f_o of the VCO. When V_i is applied, the PLL should operate in the locked condition, with f_{osc} exactly equal to f_i. The locked condition can easily be verified by observing V_i and V_{osc} simultaneously on a dual-trace oscilloscope. If $f_i = f_{osc}$, stable waveforms of both V_i and V_{osc} can be observed. Otherwise, one of the waveforms on the scope screen is blurred or is moving with respect to the other.

By changing f_i of the incoming signal, determine the actual lock range of the PLL, i.e., determine the maximum and the minimum frequency f_i such that starting from the locked condition the PLL remains in the locked condition. The lock range should be equal to f_{max} - f_{min}. When the peak-to-peak

amplitude of the incoming signal V_i is minimum, the PLL remains locked.

The PLL is composed by the 64 HCMOS divider (CMOS 4046), an LM358 operational amplifier working. The loop is stable and the lock is fast, also owing to the high value of the frequency used as reference. The module shouldn't require any tuning, verify only the voltage on pin 1 of the 74HC393 IC, it should be about 2 V with no input signal. The minimum input signal required is about 2Vpp. The lighting of a LED indicates the PLL LOCK condition.

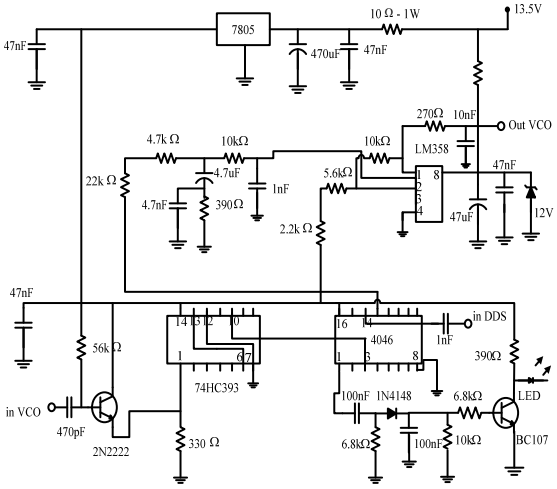

Fig. 10 Circuit diagram of PLL using CMOS 4046

VI. Simulation Results of PLL Components

PLL module is simulated by using CD4046 IC and measured by LED that indicate lock condition and unlocked condition. The higher the reference frequency from the DDS is, the faster the lock condition.

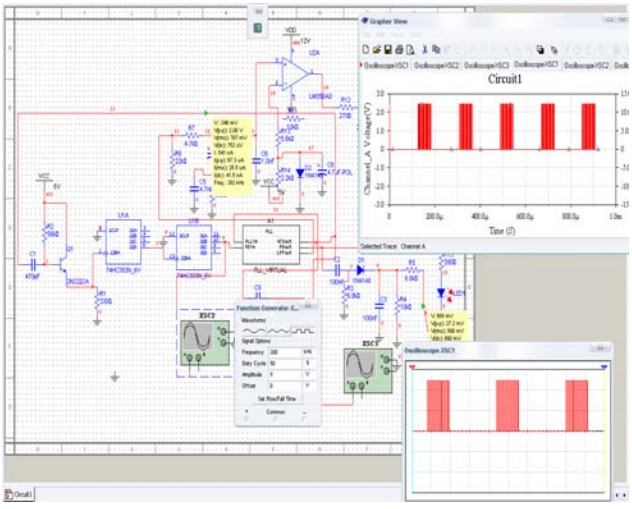

Fig. 11 Unlocked condition stage

The lock condition stage is reached by using the reference frequency 2MHz from giving function generator and run time up to 100μs. Lock condition is shown by LED.

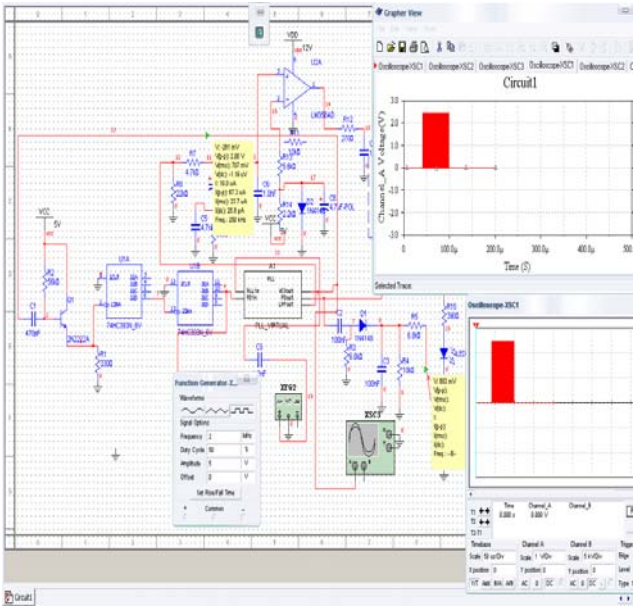

Fig. 12 Lock Condition Stage

Fig. 13 shows the 64 divider of 74HC393IC output waveform. The VCO output is then input to the 64 divider and its frequency waveform is viewed by graphic viewer. The 64 divider output is caught by oscilloscope.

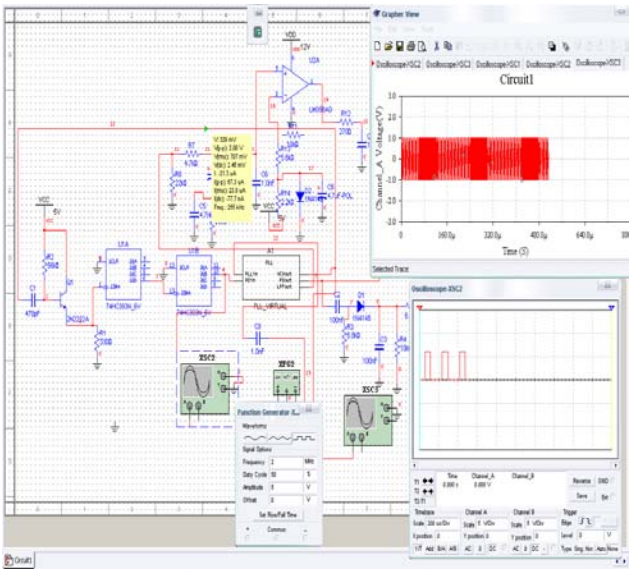

Fig. 13 74HC393 Output Waveform

VII. Test Results of PLL Module

The output of the PLL at pin 4, built in VCO output, is square waveform and is then input to the 74HC393 that input frequency is divided by 64. This output frequency is then input to the phase detector at pin 3. When the output of the phase detector in 4046 matches the reference frequency at pin 14, the 4046 output pin is not output signal. This stage shows lock condition. The test result of the square waveform of VCO

output is shown in Fig. 14. The PLL of VCO output result is square waveform and its frequency nearly 2MHz and output voltage is 5 volts. The unlock condition is taken place between reference frequency 20kHz and 350kHz and lock condition is tested under 20kHz and up to 350kHz.

Fig. 14 PLL CD4046 of VCO output waveform

VIII. Discussions and Conclusions

In this paper, the voltage control oscillator produces the required frequencies ranges from 12.5 MHz to 39 MHz so that CMOS 4046 PLL IC build in VCO is used because it is available the required frequencies ranges. The external components R_1 and R_2 are adjusting the VCO ranges. The frequency range of CD 4046 IC is considered from 12.5 MHz up to 17 MHz.

However, the generated frequency of CMOS 4046 PLL IC is nearly 2 MHz to 3 MHz. If the needed components are achieved, the reference input frequency for PLL can feed to get exactly. In this design, NE 602, BF324, BF244 and varicap diodes such as MVAM 115/ BB112 are required when constructing the voltage control oscillator to produce required frequencies ranges from 12.5 MHz to 39 MHz.

The local oscillator as PLL module, consisting of prescalar as 74HC393 IC is used for prescalar, CMOS4046 PLL IC used as phase detector, loop filter and voltage control oscillator, is constructed by using direct digital synthesizer technology.

Acknowledgment

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